REMARKS

The undersigned attorney and Examiner Li conducted a telephonic interview on January 10, 2007. The undersigned thanks the examiner for her time and comments during the Examiner's interview.

During the Examiner's Interview, the claims and the cited art were discussed. The examiner acknowledged that U.S. Patent No. 4,816,913 to Harney et al. does not disclose the feature: "the field [of a local register instruction] representing a mask in which each bit of the mast identifies a different byte of the destination register," as recited, for example, in independent claim 17. The examiner further indicated that the current rejections, as presented in the October 31, 2006, Office Action, will be withdrawn. No other agreement regarding the claims was otherwise reached.

As requested by the examiner, and for the sake of completeness, applicant's comments regarding the examiner's rejections are provided herein.

Claims 17-21, 23-26 and 28-29 are pending in the above-referenced patent application. Claims 17 and 26 are independent.

The examiner rejected claims 17-21, 23-26 and 28-29 under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 5,663,012 to Shimizu et al., in view of the reference "Programming, Compiling and Executing Partially-Ordered Instruction Streams on Scalable Shared-Memory Multiprocessors" by D. K. Probst (hereinafter Probst), and further in view of U.S. Patent No. 4,816,913 to Harney et al.

The examiner also rejected claims 17-21, 23-26 and 28-29 under 35 U.S.C. §103(a) over the reference Computer Systems Design and Architecture by V. P. Heuring and H. F. Jordan (hereinafter Heuring), in view of Probst, and further in view of Harney.

Specifically, in relation to independent claim 17, the examiner admitted that "Shimizu has not taught the field representing a mask in which each bit of the mask identifies a different byte of the destination register. The examiner, however, contended that:

> Harney has taught the field representing a mask in which each bit of the mask identifies a different byte of the destination register (Harney column 40, lines 40-50 and Figure 12A). Shimizu has taught that the instructions store the results in a specific location in the destination (Shimizu column 4, line 51 to column 5, line 40), but has not taught the specifics of how

> these instructions work. In other words, Shimizu has not taught how the instructions specifically designate the destination location, just that the destination location is designated. Harney has taught that the mask designates the destination location where a result is stored (Harney column 40, lines 40-50 and Figure 12A). A person of ordinary skill in the art at the time the invention was made, and as recognized by Harney, would have recognized that the mask of Harney prevents erroneous data from being written into a destination location (Harney column 41, lines 6-7). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the mask of Harney in the device of Shimizu to prevent erroneous data from entering memory. (Office Action, Page 5, Paragraph 8)

Applicant's independent claim 17 recites "a local register instruction that loads one or more bytes, specified by a multiple-bit field of the instruction, within a local destination register with a shifted value of another operand, the field representing a mask in which each bit of the mask identifies a different byte of the destination register."

Harney, on the other hand, describes a processor for expanding a compressed video signal with a pixel interpolator that interpolates between input pixel values in two dimensions (Abstract). Harney explains, in relation to FIG. 2, that data held in a FIFO output buffer 236 is provided to a video random access memory (VRAM) 216. With respect to FIFO output buffer 236, Harney explains:

> **FIG. 12A is a block diagram showing circuitry suitable for use as the output FIFO 236. ...**
>
> ...
>
> **If a signal OFR, provided by a flip-flop 1232 has a logic-zero value, indicating that no memory write operation is in progress for the output FIFO 236, the control circuitry 1216 pulses a signal LOR to transfer the value in the register 1220 to the output register 1218 and to transfer a four-bit byte mask held in a latch 1228 into a four-bit register 1230. One-half of one period of the signal CK after the control circuitry pulses the signal LOR, it pulses a signal WR which is applied to the set input terminal, S, of the flip-flop 1232. This action changes the state of the signal OFR, provided by the flip-flop 1232 to a logic-one value.**
>
> **The signal OFR is applied to the VRAM control unit 238 via the bus R/S. A value of logic-one from the signal OFR is interpreted by the VRAM control unit 238 as a request for a VRAM write operation using the address value held in the VRAM control unit for the output FIFO 236 and using the 32-bit data value held in the register 1218. The byte mask in the register 1230 is applied to the VRAM control unit 238 via the bus CASM. This mask is used in the VRAM control unit 238 to condition the VRAM 218 to store only those bytes in the register 1218 having byte positions that correspond**

> **to the byte mask signal CASM, that is, only those bytes which were marked as valid by the control circuitry 1216 as they were loaded into the register 1220. The method by which bytes are marked as valid and the use of the signal CASM by the VRAM control unit 238 are described in detail below. (col. 39, line 59, to col. 40, 50)**

Thus, in Harney the byte mask is held in a register 1230. Therefore Applicant contends that the byte mask is not an instruction field forming part of an instruction. Further, Harney explicitly states that "[t]his mask is used in the VRAM control unit 238 to condition the VRAM 218 [*sic – should be VRAM 216*] to store only those bytes in the register 1218 having byte positions that correspond to the byte mask signal CASM" (col. 40, lines 42-45). In other words, the byte mask identifies bytes positions in a source register (specifically, register 1218) whose content are selected and subsequently stored in the VRAM 216. Therefore, the byte mask is not used to identify byte position in a destination register (i.e., the byte positions into which content will be loaded). Accordingly, Harney fails to disclose or suggest at least "the field representing a mask in which each bit of the mask identifies a different byte of the destination register," as required by applicant's independent claim 17.

As acknowledged by the examiner, Shimizu also fails to disclose or suggest at least the feature of "the field representing a mask in which each bit of the mask identifies a different byte of the destination register." Indeed, Shimizu's GETxx and PUTxx instructions do not use masks to specify the particular locations of the source or destination operands. Rather, each individual GETxx and PUTxx instruction causes data transfer from specific bytes of a source operand to specific bytes of a destination operand. As such, Shimizu's instructions have no need to use masks to identify which bytes of the operands are involved in the data transfer operation because the specific bytes of the source and destination operands affected by operations of Shimizu's instructions are implicitly identified by the instructions themselves. If it is desired to load data from different byte locations of the source, or into different bytes of the destination operand, it is necessary to execute different GETxx or PUTxx instructions to accomplish that.

With respect to the other references relied upon by the examiner to reject claim 17 (namely, Heuring and Probst), Heuring describes a RISC computer architecture and corresponding instruction set. For example, Heuring describes at pages 150 and 159-161, a shift instruction *shr*. As shown in the SRC Instruction Set summary (no page number available), none

of the listed instructions includes mask that is used to identify different bytes of a register. Furthermore, as described in the Instruction Set Summary, the instruction *shr ra, rb, c3*, causes the processor to "shift rb right into ra by constant shift count c3 ≤ 31". As more particularly explained in Heuring's Table 4.5 and Table 4.10, on pages 150 and 160, respectively, the last step T7 in the execution of *shr* instruction causes the value of the operand C, which holds the shifted value held in *rb*, to be loaded into the destination register *ra* in its entirety. Thus, none of the various embodiments of the instruction *shr* as described by Heuring causes the value of an operand to be loaded into one or more bytes of a destination register as specified by a mask, as required by applicant's independent claim 17. Thus, Heuring does not disclose or suggest at least the features of "the field representing a mask in which each bit of the mask identifies a different byte of the destination register," as required by applicant's independent claim 17.

Probst discusses the performance of a large-scale shared-memory multi-processor architecture. Probst, however, does not discuss specific instructions forming the multi-processors' instruction set, and therefore does not describe instructions that load one or more specified bytes within a local register with a shifted value of another operand using a multiple-bit mask included in the instructions. Accordingly, Probst also does not disclose or suggest at least the features of "the field representing a mask in which each bit of the mask identifies a different byte of the destination register," as required by applicant's independent claim 17.

Because none of Shimizu, Heuring, and Probst and Harney discloses or suggests, alone or in combination, at least the features of "the field representing a mask in which each bit of the mask identifies a different byte of the destination register," applicant's independent claim 17 is therefore patentable over the cited art.

Claims 18-21, 23 and 24 depend from independent claim 17 and are therefore patentable for at least the same reasons as claim 17.

Independent claim 26 describes an apparatus featuring "a command that causes the ALU to load one or more bytes, specified by a multiple-bit field of the command, within a destination register of a selected microengine with a shifted value of another one or more bytes of a source register, the field representing a mask in which each bit of the mask identifies a different byte of the destination register." For similar reasons as those provided with respect to independent claim

17, at least these features are not disclosed by the cited art. Independent claim 26 is therefore patentable over the cited art. Claim 28-29 depend from claim 26, are therefore patentable for at least the same reasons as independent claim 26.

It is believed that all the rejections and/or objections raised by the examiner have been addressed.

In view of the foregoing, applicant respectfully submits that the application is in condition for allowance and such action is respectfully requested at the examiner's earliest convenience.

All of the dependent claims are patentable for at least the reasons for which the claims on which they depend are patentable.

Canceled claims, if any, have been canceled without prejudice or disclaimer.

Any circumstance in which the applicant has (a) addressed certain comments of the examiner does not mean that the applicant concedes other comments of the examiner, (b) made arguments for the patentability of some claims does not mean that there are not other good reasons for patentability of those claims and other claims, or (c) amended or canceled a claim does not mean that the applicant concedes any of the examiner's positions with respect to that claim or other claims.

Please apply any required fees to deposit account 06-1050, referencing the attorney docket number shown above.

Respectfully submitted,

Date: Jan 11, 2007

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